IN THE SPECIFICATION

Please replace the paragraph from page 6, line 26, to page 7, line 13, with the following replacement paragraph.

In a preferred embodiment of the present invention, there is provided a controller system having a relatively high performance master processor, and a relatively low performance slave processor all interconnected by a bus subsystem. The slave processor is disposed relative to the memory such that it experiences less read latency and uses less bus bandwidth during memory accesses than the master processor. In a particularly preferred embodiment of the present invention, the slave processor is embedded in a bridge device of the bus subsystem[.] located closer to the memory. In use, the slave processor alleviates the burden of memory accesses otherwise imposed on the master processor. Thus, much of the cycle time of the slave processor is stalled on memory accesses. The slave processor therefore need not be especially sophisticated or fast.

Please replace the paragraph at page 8, lines 15-24, with the following replacement paragraph.

The slave processor can also improve system performance in performing other management tasks associated with the device interface chips. For example, the slave processor can be instructed to [t] construct requests to device interface chips and handle data produced on execution of such requests by the device interface chips. In this arrangement, only abbreviated information need be communicated between the salve processor and the main processor. Thus traffic on the intervening bus subsystem can be reduced.

Please replace the paragraph from page 9, line 21, to page 10, line 6, with the following replacement paragraph.

Referring first to Figure 1 an example of a data processing system of the present invention comprises a master processor 10 coupled to a bus subsystem 20. The bus subsystem 20 is also coupled to a memory 50 via a bridge device 40. A slave processor 30 is also connected to the bus subsystem 20 ~~30~~. The master processor 10 may be implemented by a microprocessor

such as a PowerPC processor 750 available from International Business Machines Corporation operating at a clock frequency of 400MHz. The slave processor 30 may also be implemented by a microprocessor such as a PowerPC processor 403 available from International Business Machines Corporation operating at a clock frequency of 100MHz.